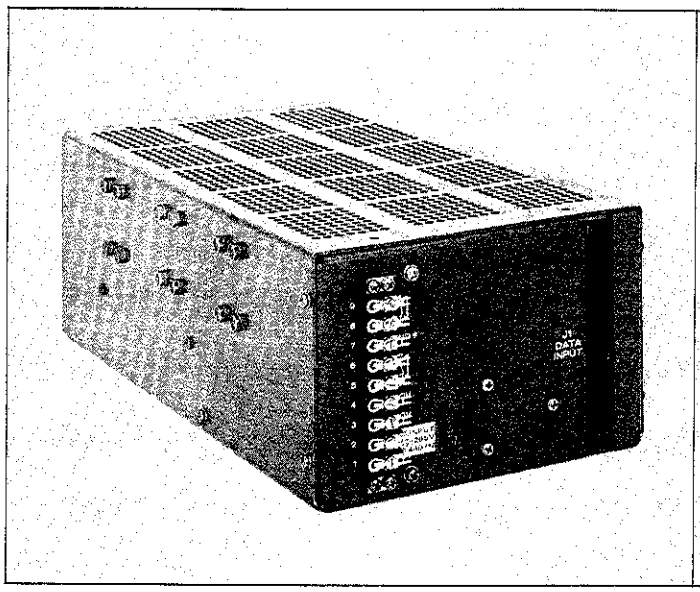
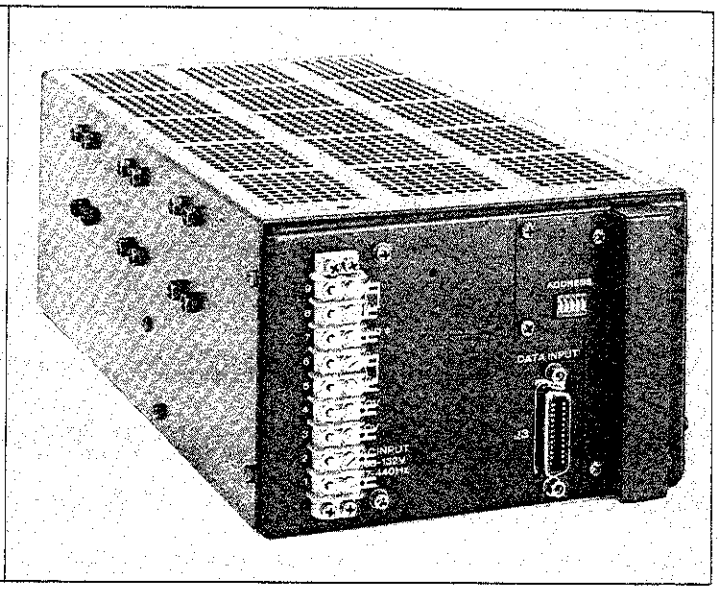
Lambda LF series





Features

LF-9-04	LF-9-04-GPIB
8, 12, or 24 bit BCD programming or ASCII programming	IEEE Standard 488-75 interconnector bus ASCII programming
0.01% regulation, line or load	0.01% regulation, line or load
A 2 msec programming time for full voltage compliance	A 2 msec programming time for full voltage compliance
15 mV accuracy for 50 V BCD programming 30 mV accuracy for 50 V of ASCII programming	30 mV accuracy for 50 V of ASCII programming
Resolution 50 mV [BCD] at 50 V; 100 mV for ASCII	Resolution 100 mV at 50 V
100% sinking capability	100% sinking capability
Ripple-10 mV pk-pk [BCD] on 50 Volt range; 20 mV for ASCII optical isolation	Ripple-20 mV pk-pk on 50 Volt range
Current limit flag	Optical isolation
Busy ready flag	Current limit programming
Current limit programming	Service request
Current over-ride	Worst-case overshoot-1 volt
Zero over-ride	Transient response-1.2 msec
Inverted/noninverted input	Unique digital circuitry designed with CMOS and TTL
Zero adjust	
Worst-case overshoot-1 volt	
Transient response-1.2 msec	
Unique digital circuitry designed with CMOS	

Ordering Information

Model LF-9-04	Price $1981	Model LF-9-04-GPIB	Price $2375

Specifications—LF-9-04

DC output

Volt (VDC)	MAX AMPS AT AMBIENT OF: 40°C	50°C	60°C
0 to ±49.95	1.98	1.8	1.6

Output Range
X1 range: ±9.99 V in 10 mV steps
*X5 range: ±49.95 V in 50 mV steps
X10 range: ASCII only—selected automatically (0- to ±49.9 V in 100 mV steps

Source or sink
1.98 amps continuous

Regulated Voltage
regulation line .....0.01%—for line variations 105-132 VAC (see AC input option)
regulation load (all ranges) .....0.01%—for load variation of 0 to full load
ripple and noise .....X1 range: 2.0 mV pk-pk max
*X5 range: 10 mV pk-pk max
X10 (ASCII): 20 mV pk-pk max
temperature coefficient .....Voltage
X1 range: .005%/°C + 35 μV/°C
*X5 range: .005%/°C + 0.115 mV/°C
X10 range: (ASCII only) .005%/°C + .215 mV/°C
Current
All ranges: 500 μA/°C

Constant Current Operation
Current range: 1% to 99% of full scale
Regulation line .....1 mA max
load .....20 mA max

AC Input
105-132 VAC, 47-440 Hz. For 187-242 or 205-265 VAC see AC input option.

Ambient Operating Temperature Range
Continuous duty from 0° to 60°C with load current ratings shown in table.

Storage Temperature Range
−55°C to +85°C

Basic Accuracy
(at 25°C, 115 VAC input and no load) .....Voltage
X1 range: 3 mV
*X5 range: 15 mV
X10 range: 30 mV (ASCII only)
Current
All ranges: 10 mA

Resolution .....Voltage
X1 range: 10 mV
*X5 range: 50 mV
X10 range: 100 mV (ASCII)
Current
All ranges: 20 mA

Transient Response
1.2 msec to within .05% of full scale for 90% load change

*BCD only

Overshoot
Worst case overshoot 1 volt under any conditions.

Input Data Word
A 24 Bit data word is used comprising of 12 bits BCD voltage programming, 8 bits BCD current and one bit each for gain, polarity and current limit override. Data word may be accepted in 3, 2, or 1 sequential segments of 8, 12, 24 bits, or ASCII to make up the 24 bits. Current is programmed as a percentage of full scale.

Programming Time
See graphs on page 104.

Data Validity
10 μsec

Data Loading
Logic Levels—all 0 to +5V. One CMOS load per line.
Compatible with TTL or DTL
Interface requirements:
CMOS—direct
DTL—direct
TTL—direct, with a 10K pull up resistor on each data line to +5 V bus.

Control Lines
One TTL or DTL buffer per line
Data Flag—CMOS input
Zero Override—requires sinking of 15 mA, compatible with DTL or TTL buffers
Final Transfer Pulse—CMOS input

Output Flags
1. Current Limit Flag—optical coupler, conducting when in current limit.
2. Busy Ready Flag—open collector, logic zero when ready to accept new data.

Cooling
Convection-cooled, no heatsinks or blower necessary.

Mounting Positions
One mounting position on horizontal plane.
Input/output connections through heavy duty barrier strip and connector

Physical Data

Model	Size (Inches)	Weight Lbs. Net	Lbs. Ship
LF-9-04	4-15/16 x 7-1/2 x 14	20	22

Options
AC Input

Add Suffix	For Operation at:	Add to Price
—V	187-242 VAC, 47-440 Hz	12%
—V_1	205-265 VAC, 47-440 Hz	12%

Accessories
Rack adapters LRA-15, LRA-17. Overvoltage protectors, chassis slides, blank panels. See pages 66-68.

Guaranteed for 5 years
5-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

Specifications—LF-9-04-GPIB series

DC Output

Volt (VDC)	MAX AMPS AT AMBIENT OF: 40°C	50°C	60°C
0 to ±49.95	1.98	1.8	1.6

Output Range
X1 range: ±9.99 V in 10 mV steps
X10 range: Selected automatically (0- to ±49.9 V in 100 mV steps)

Source or Sink
1.98 amps continuous

Regulated Voltage
regulation line .....0.01%—for line variations 105-132 VAC (see AC input option)
regulation load (all ranges) .....0.01%—for load variation of 0 to full load
ripple and noise .....X1 range: 2.0 mV pk-pk max
X10: 20 mV pk-pk max
temperature coefficient .....Voltage
X1 range: .005%/°C + 35 μV/°C
X10 range: .005%/°C + .215 mV/°C
Current
All ranges: 500 μA/°C

Constant Current Operation
Current Range: 1% to 99% of full scale
Regulation line .....1 mA max
load .....20 mA max

AC Input
105-132 VAC, 47-440 Hz. For 187-242 or 205-265 VAC see AC input option.

Ambient Operating Temperature Range
Continuous duty from 0° to 60°C with load current ratings shown in table.

Storage Temperature Range
−55°C to +85°C

Basic Accuracy
(at 25°C, 115 VAC input and no load) .....Voltage
X1 range: 3 mV
X10 range: 30 mV
Current
All ranges: 10 mA

Resolution .....Voltage
X1 range: 10 mV
X10 range: 100 mV
Current
All ranges: 20 mA

Transient Response
1.2 msec to within .05% of full scale for 90% load change.

Overshoot
Worst case overshoot 1 volt under any conditions.

Input Data Format
Data is entered in bit-parallel, byte-serial format as specified by IEEE Std. #488. The 24 programming bits contain 12 bits BCD voltage programming, 8 bits BCD current programming and one bit each for gain, polarity and mode. The valid data format is ASCII.

Programming Time
See graphs on page 104.

Data Loading
Logic levels ("O" ⩾ + 2.OV; "1" ⩽ + 0.8 V) and interface requirements are as specified in IEEE Std. #488.

Data Input Lines
DIO-1 thru 8 as specified in IEEE Std. #488.

Control Lines
ATN, EOI, IFC, NRFD, NDAC, DAV, SRQ, REN* as specified in IEEE Std. #488. All control and data input lines are accessed through 24-pin GPIB connector on back panel. The SRQ line is activated by a current overload condition while in constant voltage mode or overvoltage limit condition while in constant current mode. Mode of operation programmed with mode bit.

*REN is not a usable function for the LF-GPIB and is terminated in a logical "O".

Cooling
Convection-cooled, no heatsinks or blower necessary.

Mounting Positions
One mounting position on horizontal plane.
Input/output connections through heavy duty barrier strip and connector.

Physical Data

Model	Weight Lbs. Net	Weight Lbs. Ship	Size (Inches)
LF-9-04-GPIB	20	22	4-15/16 x 7-1/2 x 14-5/8

Options
AC Input

Add Suffix	For Operation at:	Add to Price
—V	187-242 VAC, 47-440 Hz	12%
—V_1	205-265 VAC, 47-440 Hz	12%

Accessories
Rack adapters LRA-15, LRA-17. Overvoltage protectors, chassis slides, blank panels. See pages 66-68.

Guaranteed for 5 years
5-year guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 5 years.

UL - Recognized

Specifications—LF-9-04-GPIB Cont'd

Summary Of The IEEE Std. #488:

IEEE Standard #488 specifies a system for the interconnection of as many as 14 pieces of test equipment on a single 24-wire bus controlled by a central processing unit. The bus consists of 8 bidirectional data lines, 8 command lines and 8 ground lines. Data is transferred along the bus via a specific 3-wire "handshake" process. This process greatly reduces the possibility of lost data since any one operation must be confirmed by all addressed units before the following operation may commence.

The address system allows the controller to identify the units which are to transmit or receive data while allowing the other units on the bus to function uninterrupted. The service request (SRQ) line provides each module on the bus with the ability to inform the controller if a particular condition in that module warrants attention or service.

Listed below are the designations of the 8 command lines and a brief function description for each:

1. ATN (ATTENTION)—This line is used to call the attention of all units on the bus (i.e., all units are listening). All command instructions must be given under this signal.
2. IFC (INTERFACE CLEAR)—This line is used to set the interface—parts of which are contained in all units on the bus—at a known quiescent state.
3. SRQ (SERVICE REQUEST)—This line provides a means for each unit on the bus to indicate to the controller that a condition exists which may require attention or service.
4. EOI (END OR IDENTIFY)—This line is used to indicate the end of a particular multiple-byte transfer sequence.
5. REN (REMOTE ENABLE)—This line is used to select between two alternate sources of device programming data (i.e., computer control or local control).

The remaining three commands comprise the three-wire "handshake" process. This process utilizes interlocking command sequences to transfer each data byte across the interface. These sequences can only proceed at the rate of the slowest addressed unit on the bus, thus assuring that all units on the bus can completely assimilate the data.

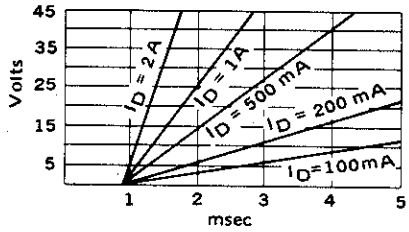
6. DAV (DATA VALID)—This command is used by the "talker" to indicate that the data on the DIO signal lines is valid and ready to be processed.
7. NRFD (NOT READY FOR DATA)—This line is used by the "listeners" on the bus to indicate whether or not they are ready to process the next byte of data.
8. NDAC (NOT DATA ACCEPTED)—This line is used by the "listeners" on the bus to indicate that the data on the line has been processed and can now be removed.

Consult Factory For:

A. Application information using BCD as input format.
B. Application information using IFC as an emergency shutdown.

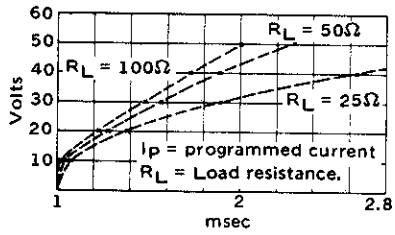
Specifications—LF-9-04, LF-9-04-GPIB cont'd

Programming Time mSec Vs Programmed Voltage Step (Constant Current Load)

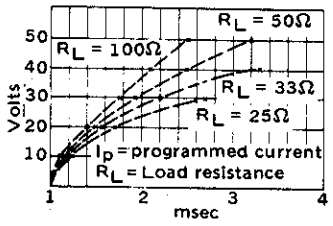


I_D = DIFFERENCE BETWEEN PROGRAMMED CURRENT AND LOAD CURRENT APPLIES TO CONSTANT CURRENT NON-CAPACITIVE LOAD

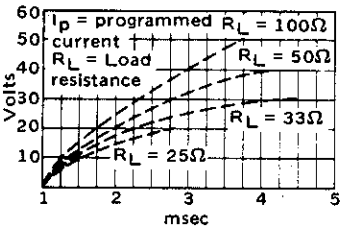
Programming Time mSec Vs Programmed Voltage Step (Resistive Load)



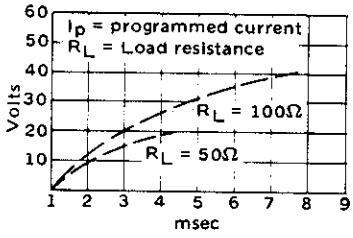
I_P = 2.0A
100% Full Load



I_P = 1.5A
75% Full Load

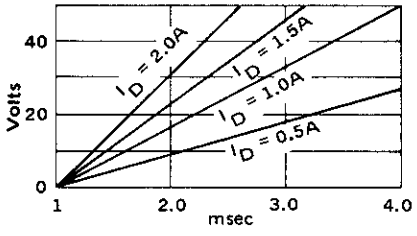


I_P = 1.0A
50% Full Load

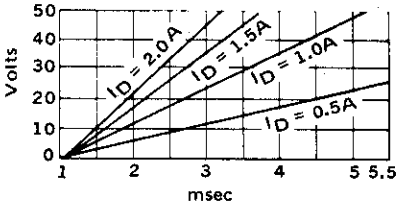


I_P = 0.5A
25% Full Load

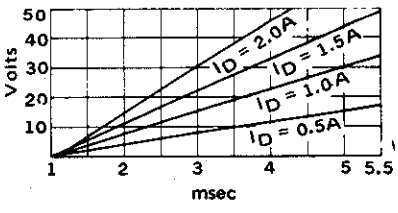
Programming Time mSec Vs Programmed Voltage Step (Capacitive Load)



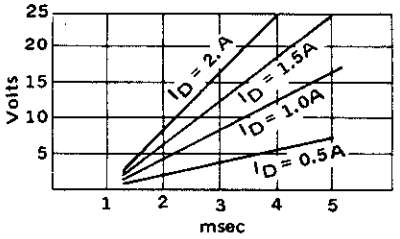
C_L = 25 mfd
Load Capacitance



C_L = 50 mfd
Load Capacitance



C_L = 100 mfd
Load Capacitance



C_L = 200 mfd
Load Capacitance

I_D = Difference between programmed current and constant load current.

DEFINITION OF TERMS:

Resolution:
Minimum programmable change.

Basic Accuracy:
Maximum deviation from programmed value at 25° C constant temperature, 115 VAC and no load.

Programming Time:
Time, after data entry, required for the supply to settle within 0.05% full scale.

Data Flag: (Not Applicable to GPIB)
Customer generated 3.3μsec minimum pulse, beginning at least 2 μsec after data is presented, to signal that data is available and ready for processing.

Final Transfer Pulse: (Not Applicable to GPIB)
Customer generated 2 μsec minimum pulse beginning at least 300 μsec after first data flag, to transfer data from input shift register into storage and the DAC's. This pulse is internally generated by the system for ASCII.

Data Validity: (Not Applicable to GPIB)
Minimum time for which data must remain present after data flag.

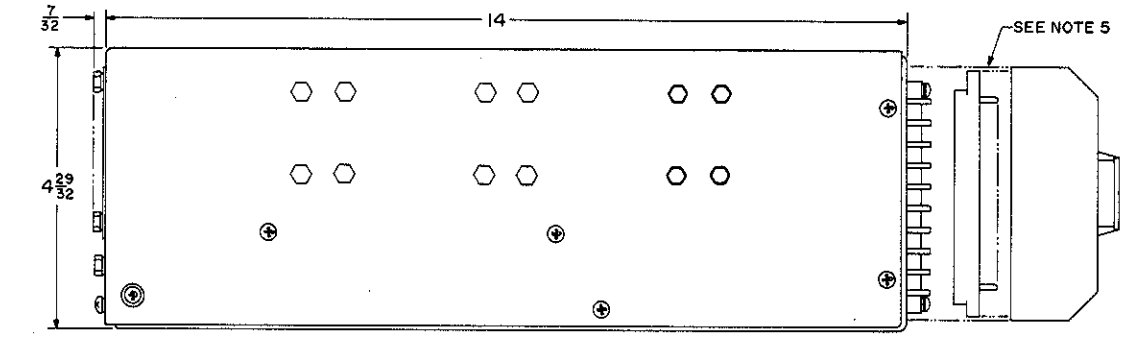
Transient Response:
Time required for supply to return to within 0.05% full scale of programmed value, for 90% change of load.

Overshoot:
Magnitude of voltage by which output may exceed programmed value or fall below zero volts during turn-on, turn-off, voltage to current limit crossover or current limit to voltage crossover and programming.

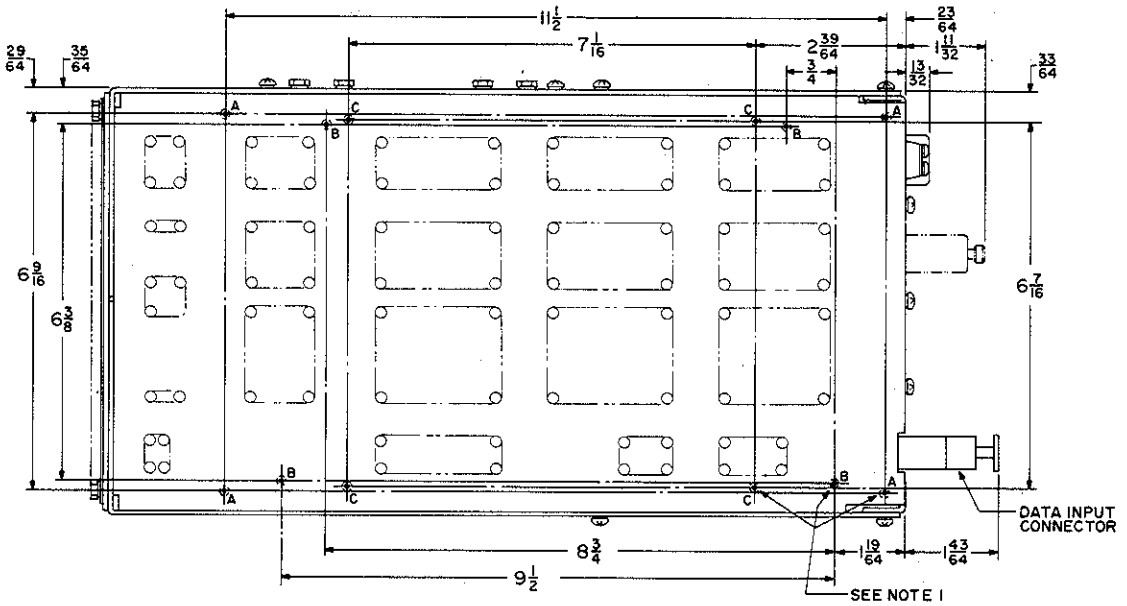
Zero Override: (Not Applicable to GPIB)
Input signal pulse programs output of power supply to zero volts. This signal is also activated when input data plug is pulled out. Zero override is a system feature that may be utilized in an emergency by forcing the output to zero volts from any previous state. When in that mode the output will be kept at zero ±50 mV max. While the output ripple will be limited to 15 mV pk-pk max.

Output Flags:
System generated signal, available to the user through the input data connector.

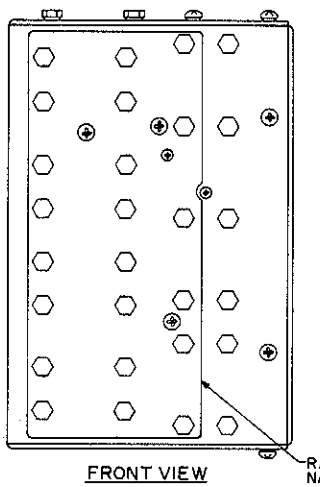
PART IV—DIMENSIONAL DRAWINGS
LF-9-04, LF-9-04-GPIB POWER SUPPLIES



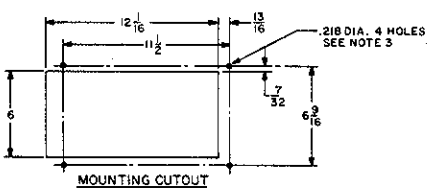
SIDE VIEW



BOTTOM VIEW



FRONT VIEW

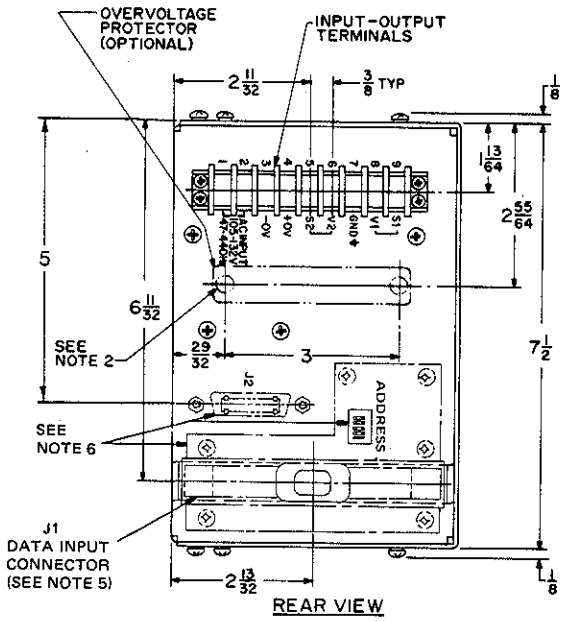


MOUNTING CUTOUT

NOTES:

1. "A" HOLES – 8-32 TAPPED HOLES (4) ON BOTTOM SURFACE FOR MOUNTING IN LRA-11 RACK ADAPTER AND FOR CUSTOMER CHASSIS MOUNTING.
   "B" HOLES – 8-32 TAPPED HOLES (4) ON BOTTOM SURFACE FOR MOUNTING IN LRA-10 RACK ADAPTER.
   "C" HOLES – 8-32 TAPPED HOLES (4) ON BOTTOM SURFACE FOR MOUNTING IN LRA-13 RACK ADAPTER.
2. TWO 6-32 TAPPED HOLES FOR MOUNTING OVERVOLTAGE PROTECTOR.
3. CUSTOMER MOUNTING SCREWS TO BE 3/8 LONG PLUS THICKNESS OF MOUNTING SURFACE.
4. CUSTOMER MUST PROVIDE CUTOUTS IN HIS MOUNTING SURFACE TO CLEAR VENTILATION PATTERNS AND ALLOW FREE AIR CIRCULATION.
5. DATA INPUT CARD EDGE CONNECTOR AND CONNECTOR HOOD KIT TO BE SUPPLIED BY LAMBDA. FOR MDL LF-9-04 ONLY.
6. DATA INPUT CONNECTOR J2, ADDRESS SWITCH AND COVER SHOWN SUPPLIED FOR LAMBDA MODEL LF904-GPIB

TERMINAL STRIP
SCREW SIZE
5-40 X 1/4



REAR VIEW